MICROCONTROLLER-BASED MULTI-FORMAT VIDEO AGC/SYNC LOOP REGULATOR PROJECT MANUAL

INTRODUCTION

The video signal contains specified AGC level parameters and composite synchronizing signal parameters that are essential for the proper processing of the video data for viewing. In some instances, these parameters may become distorted or weakened because of external interference, inadequate transmission apparatus and techniques, and other forms and/or sources of video signal degradation. In such instances, it is necessary to strengthen and/or reestablish the proper AGC level parameters and the composite synchronizing signals by incorporating various signal-processing techniques. The Microcontroller-Based Multi-Format Video AGC/Sync Loop Regulator is a project in which AGC level and composite sync signal processing techniques with practical applications are examined. In the provided applications and exercises, the experimenter explores theoretical circuit and program variations of an apparatus that modifies and/or regulates AGC levels and sync signal content and parameters of a video signal. Observations of various waveforms produced and processed throughout the circuit are essential to the development of a solid knowledge base. It is therefore assumed that the experimenter has an intermediate knowledge of video technology theory, electronic assembly (thru-hole and surface mount), electronic test equipment use (including DVM's and oscilloscopes) and AVR® RISC microcontroller programming. It should be noted at this time that all of the project variations described in this manual require a Windows operated desktop computer and an Atmel® STK500 microcontroller starter kit (available for less than $100.00) for programming the Atmel® AVR® RISC microcontrollers used in this project.

This manual is divided into three sections. The first section begins with the detailed descriptions of the various printed circuit board configurations and of each respective schematic diagrams. This description also includes equipment, tools and parts lists. Each part of the parts list is referenced to a recommended supplier or vendor. There is also a supplier/vendor listing for equipment, parts and tools at the end of this manual. The assembly procedure is to follow the printed circuit board configurations with reference to the parts list and observing the proper orientation of parts with specific keying and polarization.

The second section is an overview of the various video synchronizing techniques of the ATSC, NTSC, PAL and SECAM standards. These standards are further divided into standard definition (SD) and high definition (HD) formats with a

variety of available aspect ratios. Although this topic is deserving of an entire book, this brief tutorial section is presented in a manner that relates directly to the application of this project. It is also necessary to cover the topics of AGC level parameters and DC restoration, which are also components of the techniques presented in this project, in this section. There is a bibliography for suggested reading and reference at the end of this manual.

The third section of this manual covers the theory of operation, actual operation, programming and testing. This section is further divided into three subsections of A, B and C. Subsection A is concerned with the signal processing steps performed by the circuit from a theoretical point of view. It is in this part of the text that all of the reference and test points will be designated. The experimenter is encouraged to assign additional reference and test points of his or her design. Subsection B is an analysis of the example program that is fully applicable to the NTSC SD (4:3 aspect ratio) and the PAL/SECAM SD (4:3 aspect ratio) standards. The analysis will consist of citing the basic subroutines, which are similar to each other in structure. These subroutines are repetitive, thus forming "loops" which systematically advances and retards within the program. The steps of the program are referenced to the appropriate signal processing steps as defined in Subsection A. The individual is encouraged to use the necessary instructions and techniques applicable to AVR® RISC microcontrollers that facilitate the incorporation of these sub-routines in the example program into their own programs. Subsection C unifies all of the concepts and ideas presented in all of the previous sections and subsections into a coherent comprehension of the projects function and objective. This is accomplished by the observation and analysis of the project under actual operating conditions. The reference and test points defined in Subsection A are now used for various measurements to compare with ideal and theoretical predictions of performance as defined by the program as outlined in Subsection B. These measurements include voltage, time, propagation delay and phase difference using the recommended dual channel oscilloscope.

Upon completion of the project, the experimenter will be able to program the project to manipulate AGC levels and synchronizing signal content in any manner desired. This indicates that not only is the project capable of producing an AGC/sync regulated video signal within established parameters of a selected video format and standard, but has the potential of encoding video signals. This encoded video signal would then be decoded by another project with a proper program for decoding. This opens a variety of experimental applications of the project for exploration by the experimenter.

SECTION ONE-PROJECT OVERVIEW

This project consists of a basic version and an advanced version for the experimenter to enhance existing knowledge and comprehension of video synchronizing signals as well as the introduction of new concepts and practical applications of video synchronizing signal processing techniques. Each version has a separate set of printed circuit board layouts that accompany this manual. Each set

has a top or power side and a bottom or signal side in the form of two sets of paper printouts. Transparencies are available from J.L.K. Electronics. These sets are to scale and ready for use by the experimenter to manufacture double-sided printed circuit boards (PCB). There are currently two popular methods of PCB manufacture available to the experimenter. These are the iron-on transfer method and the photo-positive method. After repeated trials of both methods by J.L.K. Electronics, the photo-positive method proved to be the superior choice. The transparencies are used in the preferred photo-positive PCB manufacturing method. In the case of the download order, the paper printouts of the PCB layouts may be copied onto transparency film. Again, after repeated trials, J.L.K. Electronics has determined that the transparencies should be made using a laser jet copier/printer with the dry toner setting at maximum. To date, ink jet or ink-based copiers/printers do not produce a transparency with perfectly opaque pads and traces. Selection of a type of transparency film for laser jet copiers/printers is of extreme importance. This type of film is made to withstand the heat generated by the copier/printer and with not wrinkle or deform. This method also requires photo-positive sensitized double-sided copper-clad boards, a glass exposure kit and a UV light source. These are all Injectorall products available from Digi-Key Corporation. The developer is a solution of approximately 12 to 15 grams of sodium hydroxide (lye) added to each liter of water. The boards must be etched, usually with an etchant such as Ferric Chloride (Radio Shack® or All Electronics Corporation). The majority of the holes to be drilled for parts placement are done with a #60 drill bit preferably using a Dremel® rotary tool with a Dremel® drill press. Both items are available at most hardware stores. Detailed instructions for making PCBs are available on-line at the Injectorall website and a similar method derived by J.L.K. Electronics is presented at the end of this section. Ready-made boards are available from J.L.K. Electronics. Please go to www.jlkelecronics.com for current availability and pricing plus shipping and handling. These are high-quality silk-screened boards specially made for J.L.K Electronics.

Each version incorporates the Atmel® ATtiny2313V microcontroller. The advanced version uses an additional microcontroller as a coprocessor whereas the basic version does not. The Atmel® ATtiny13 is the microcontroller is the preferred device. The determination of this device pair is predicated on the identical clock speed of twenty megahertz and that the ATtiny13 can be clocked from a clock output of the ATtiny2313V. This clock output is an auxiliary function of pin 6 of the ATtiny2313V. This coprocessor configuration is demonstrated to allow the experimenter to explore a diverse number of combinations of signal processing techniques. The most desirable combination is to assign the ATtiny13 the tasks of format identification, field identification and/or reference point verification and the ATtiny2313V would generate the appropriate AGC/sync processing signals. The ATtiny13 would provide output signals that would be applied to inputs of the ATtiny2313V. The ATtiny2313V program would use this output data from the ATtiny13 to select the proper video format subroutine in the program memory to generate AGC/sync processing signals of the detected format. Field identification is necessary in all cases. Both of the versions use sync separators that are interchangeable with different features, but it will be shown that the programs for each of the microcontrollers will not vary. These interchangeable sync separator

integrated circuits are the LM1881, EL1883, EL4581 and ISL59885. The LM1881 and the EL4581 sync separators are each available in a standard 8-pin DIP. The EL1883 and the ISL59885 are each available only in surface mount device (SOIC) packaging and require SOIC to DIP socket adapters which will be described later in detail. The LM1881 and the EL4581 sync separators each have a field identification output, while the EL1883 and the ISL59885 sync separators do not have a field identification output. Reference point verification is primarily concerned with verifying the accurate detection of the vertical pulse of the aforementioned sync separators or the option of programming the ATtiny13 to select another reference point. This may be accomplished by identifying the various peculiarities distributed within the vertical blanking interval. The relationship of these reference points to the vertical pulse detected by the one of the aforementioned sync separators are compared to each other. The results of this comparison are also compared with the detected video format parameters contained within the program. This configuration provides a foundation to expand on the programming skills of the experimenter in order to ensure the acquisition of accurate data for signal processing. Use of the ATtiny13 allows additional format subroutines to be placed in the flash program memory of the ATtiny2313V at the discretion of the experimenter. The ATtiny13 can be used to extract other data that is contained in the vertical blanking interval, such as widescreen signaling. Widescreen signaling and other VBI data as well as VBI peculiarities will be addressed in further detail in Section 2 and Section 3. The remainder of the integrated circuits, in each version, is identical: one CD4001; one CD4011 (or CD4093); one CD4023; one ISL4089 and; four OPA698 integrated circuits.

There is a schematic diagram for each version. There is also a diagram depicting the "actual" gating section as compared to an "ideal" gating section of the circuit. The "ideal" gating section contain the gates the project was designed. That is, the ideal design contains single gates that would require surface mount devices or SMD. The gates of the actual diagrams are configured to perform as their SMD counterparts and are contained within standard DIP packages for insertion into machine pin collet sockets. Two of the two input positive NOR gates of the CD4001 are configured to constitute a single two input positive OR gate, which is a 1G32 SMD. The CD4001 is thus configured to function as two 1G32 SMD gates or one dual two input positive OR gate, which is a 2G32 SMD. A CD4071, which is a quadruple two input positive OR gate may be substituted for the CD4001. Two of the triple three input positive NAND gates of the CD4023 are configured as a single two input positive AND gate or a 1G08 SMD. The remaining gate of the CD4023 is configured as a single inverter or a 1G04 SMD. The CD4011 is a quadruple two input positive NAND gate of which all of the gates are configured to function as a single two input exclusive OR gate or a 1G86 SMD. The CD4011 may be replaced by a CD4093, which is a quadruple two input positive NAND Schmitt trigger. The selection of these particular IC gates was predicated on several features that are advantageous to the experimenter and in accordance to design criteria. The ease of inserting and removing the IC gates, using the required machine pin collet sockets is the most obvious advantage. The machine pin collet sockets are required in order to solder proper connections to the pins on the power supply side of the printed circuit

board. The larger DIP packages also make DVM and oscilloscope measurements more accessible. Finally, all of the logic gates are in use, with no unused inputs or outputs. This is an important part of CMOS design criteria.

There are five integrated circuits, other than voltage regulators, remaining to be briefly reviewed. The four OPA698 integrated circuits are wideband voltage-limiting amplifiers manufactured by Texas Instruments® under the brand name of Burr-Brown®. The ZXFV4089 is a DC restored amplifier manufactured by Zetex. These five amplifiers are only available in the SMD packages. Another unique feature of the project is the implementation of SOIC to DIP socket adapters required for the use of these amplifiers. These adapters are manufactured by Aries® Corporation and are available from Digi-Key® Corporation. As previously stated, the EL1883 and the ISL59885 sync separators also require these adapters. Use of these adapters makes it possible to readily interchange integrated circuits of identical function and pin designation as well as accessibility of the pins for testing. The HFA1135 voltage-limiting amplifier, manufactured by Intersil®, may be used in place of the OPA698 if the experimenter wishes to evaluate the performance differences of the two amplifiers. All of the integrated circuits described in the foregoing text are available from Digi-Key® Corporation as listed in the following equipment and parts lists with the exception of the HFA1135.

1. PCB Manufacturing Equipment and Supplies
   A. Photo-Positive Method (Suggested Method)

No.	Item	Manufacturer	Vendor	Stock No.
1.	18" Fluorescent UV Lamp	Injectorall	Digi-Key®	PC557F-ND
2.	Glass Exposure Kit	Injectorall	Digi-Key®	PC-GL69
3.	4 x 6 Positive Coated Double-Sided Board	Injectorall	Digi-Key®	PC41P-ND
4.	Etchant(Ferric Chloride)		Radio Shack®	276-1535
			All Electronics	ER-1
5.	Developer (100% Lye or Sodium Hydroxide)		Any Hardware Store	

   B. Finishing Equipment

No.	Item	Vendor	Stock No.
2.	Speed Chuck for Dremel Rotary Tool	All Electronics	CHK-1
3.	Dremel MultiPro Rotary Tool	Dremel®	2851-01
4.	Dremel Work Station	Dremel®	220
5.	Drill Bit Set with assortment of sizes from #65 to #7		
6.	Steel wool soap pads		

2. Basic Version Parts

Qty	Reference Nos.	Device/Value	Vendor	Stock No.
1	IC2	ATtiny2313V	Digi-Key®	ATTINY2313-20PU-ND
1	IC8	CD4001	Digi-Key®	296-2028-5-ND
1	IC3	CD4011	Digi-Key®	296-2031-5-ND
1	IC7	CD4023	Digi-Key®	296-2041-5-ND
1	IC10	ZXFV4089	Digi-Key®	ZXFV4089N8CT-ND
4	IC4,IC5,IC6,IC9	OPA698ID	Digi-Key®	296-15860-5-ND

Qty	Reference Nos.	Device/Value	Vendor	Stock No.
1	IC1	EL1881CN	Digi-Key®	EL1881CN-ND
1	LM7805	LM7805	Digi-Key®	LM7805CT-ND
1	LM7905	LM7905	Digi-Key	LM7905CTFS-ND
1	BR1	W01G	Digi-Key®	W01GDI-ND
22	C1,C2,C3,C5,C6,C11, C12,C13,C14,C16,	0.1uf/50V Axial Ceramic OR	All Electronics	AM-104
	C17,C18,C22,C23, C25,C28,C29,C35, C37,C39,C41,C43	0.1uf/50V Axial Ceramic	Digi-Key®	399-4491-1-ND
15	C4,C7,C10,C15,C19, C20,C21,C24,C26,	4.7uf/6.3V Axial Tantalum OR	Digi-Key®	399-1453-ND
	C27,C34,C36,C38, C40,C42	4.7uf/10V Radial Tantalum	Digi-Key®	399-3619-ND
2	C8,C9	22pf/100V Mono Ceramic	Digi-Key®	P4841-ND
4	C30a,C30b,C31a, C31b	470uf/16V Axial Electrolytic	Digi-Key®	4021PHCT-ND
2	C32,C33	0.1uf/50V Mono Ceramic	Digi-Key®	P4923-ND
2	D1,D2	1N4148 diodes	Digi-Key®	1N4148DICT-ND
2	J1,J2	RCA Jacks	Digi-Key®	CP-1427-ND
1	R1	91 ohm	Digi-Key®	P91BACT-ND
4	R2,R8,R18,R21	430 ohm	Digi-Key®	P430BACT-ND
1	R3	510 ohm	Digi-Key®	P510BACT-ND
1	R4	12.0K ohm	Digi-Key®	P12KBACT-ND
1	R5	680K ohm	Digi-Key®	P680KBACT-ND
6	R6,R7,R9,R10,R11, R32	4.7K ohm	Digi-Key®	P4.7KBACT-ND
2	R12,R14	3.6K ohm	Digi-Key®	P3.6KBACT-ND
2	R13,R15	1.5K ohm	Digi-Key®	P1.5KBACT-ND
1	R16	10.0K ohm	Digi-Key®	P10KBACT-ND
2	R17,R28	1.3K ohm	Digi-Key®	P1.3KBACT-ND
3	R19,R20,R26	75 ohm	Digi-Key®	P75BACT-ND
3	R22, R27,R33	Jumper-See Text	Digi-Key®	P0.0BACT-ND
1	R23	330 ohm	Digi-Key®	P330BACT-ND
2	R24,R25	300 ohm	Digi-Key®	P300BACT-ND
1	R29	3.0K ohm	Digi-Key®	P3.0KBACT-ND
1	R30	500 ohm Pot	Digi-Key®	490-3020-ND
1	R31	1.0K ohm Pot	Digi-Key®	490-3007-ND
1	T1	12.6VCT@0.45A	Radio Shack®	273-1365
1	XTAL	20 MHz Crystal	Digi-Key®	X439-ND
6	8-Pin Machine Pin	Collet Socket	Digi-Key®	A400-ND
3	14-Pin Machine Pin	Collet Socket	Digi-Key®	A401-ND
1	20-Pin Machine Pin	Collet Socket	Digi-Key®	A404AE-ND
5	8-Pin SOIC to DIP	Adapter	Digi-Key®	A724-ND

3. Advanced Version Parts

Qty	Reference Nos.	Device/Value	Vendor	Stock No.
1	IC11	ATtiny13	Digi-Key®	ATTINY13-20PU-ND
1	8-Pin Machine Pin	Collet Socket	Digi-Key®	A400-ND
1	8-Pin SOIC to DIP	Adapter	Digi-Key®	A724-ND
1	C44	0.1uf/50V	Digi-Key®	399-4491-1-ND
1	C45	4.7uf/10V	Digi-Key®	399-3619-ND

4. Optional Replacement Devices and Accessories for Experimentation

Device/Value	Stock No.	Vendor	Replaces
CD4093	296-2068-5-ND	Digi-Key®	CD4011
EL1883IS	EL1883IS-ND	Digi-Key®	LM1881CN
EL4581CN	EL 4581CN-ND	Digi-Key®	LM1881CN
ISL59885IS	ISL59885ISZ-ND	Digi-Key®	LM1881CN
HFA1135	HFA1135IBZ	Avnet®	OPA698ID

The parts list refers R22 and R27 as jumpers and to the text. These resistor placements are for additional fine-tuning of the voltage divider subcircuit of each resistor, if the experimenter wishes to alter the AGC voltage levels, as required. D1, R27, R28, R30 and common R23 form one voltage divider subcircuit. The voltage, when active, at the common R23 is adjusted to 0.714 volts or 100 IRE. D2, R22, R29, R30 and common R23 form the other voltage divider subcircuit. The voltage, when active, at the common R23 is adjusted to 0.357 volts of 50 IRE. The program that accompanies the project does not activate either voltage divider network associated with these components. The AGC level is therefore always maintained at ground level and is only used when Pin 4 of IC10 receives an active "low" from the microcontroller. Only one of the voltage divider subcircuits should be active at any one time. Jumper R33 connects pin 11 of IC3 to pin 3 of IC4 and is shown only on the PCB layout PDF and **is NOT silk-screened on the PCB available from J.L.K. Electronics**.

The suggested minimum hand tools required for assembly are available from most hardware stores and include electronic pliers, electronic shear cutters, a nutdriver set, a precision screwdriver set and a standard screwdriver set. All of these items are produced by several manufacturers and are also available from Digi-Key® Corporation, who also is a vendor for the recommended Weller® WTCPT Soldering Station (cat no. WTCPT-ND). The recommended soldering tips are the cat. no. PTS7-ND and the cat. no. PTS8-ND. The recommended 60/40 rosin-core solder is of 0.032 diameter. Solderwick, solder flux, a vacuum desoldering tool and a small bench vise completes the minimum hand tool requirements.

A reasonably accurate Digital Multimeter and an oscilloscope are required to measure and observe the operation of the project at the assigned test points. The experimenter is encouraged to assign test point of his or her own design and compare these measurements and observations with those of this text in order to develop an independent course of experimentation and study. With this curriculum envisioned and the twenty-megahertz operating frequency of the microcontrollers as a minimum time base to be considered, a dual trace twenty-megahertz oscilloscope

would be an absolute minimum. A dual trace oscilloscope is necessary to observe the time delay between an input to the microcontroller and the associated output from the microcontroller. This observation is then compared to the calculated delay. The calculated delay is derived by adding the number of cycles of each instruction of the user program that is executed between an input event and the corresponding output event. Many of the measurements and observations of Section 3, Subsection C are predicated upon this type of comparison and procedure. An oscilloscope that is readily applicable for this project is the Tektronix™ TDS1001B oscilloscope. This is a forty-megahertz, dual channel digital storage oscilloscope with a monochrome screen and USB ports, available from Allied Electronics Inc. The stock number is 700-0174 and the current price is $850.00. The address and contact information of Allied Electronics Inc. is contained in the supplier/vendor listing at the end of this manual. Selection of a reasonably accurate Digital Multimeter (DMM) is dependent upon the individual preference of the experimenter.

The following procedures contain refinements to existing methods of photo-positive PCB manufacture. By referring to the Injectorall website it would be noticed that the refinements are applied, for the most part, to the alignment procedure. Upon inspection of the transparencies accompanying this manual or made from the printouts, the experimenter will take note of a six inch by nine inch border traversing around the four inch by six inch PCB pattern. This matches the size of the glass sheet contained in the recommended glass exposure kit. The transparencies are carefully cut around the border. After each glass exposure sheet is thoroughly cleaned, each transparency is carefully aligned and taped to one of the glass sheets in a manner so that the text on the transparency is readable through the glass sheet. This must be done by handling both each glass sheet and each transparency with extreme care to avoid leaving any fingerprints or smudges. By placing both assemblies together with one transparency in contact with the other, greater alignment accuracy may be achieved by visual means. A piece of black plastic, bakelite or some other hard material measuring five inches by eight inches by about one-half inch is obtained. This will serve as an alignment platform. Place a piece of white paper on the alignment platform. Place one of the glass sheet/transparency assemblies, glass sheet down, on the white paper. Turn off the direct lights and then turn on the yellow or red safe lights. Remove the photo positive board from the black protective bag and discard the protective sheets. Carefully align he board on the PCB pattern. This may be quite tedious. The PCB's are generally not perfectly square or exactly four inches by six inches. It is necessary to select the best two adjacent sides of the PCB to align with the two corresponding sides of the pattern. The PCB should now be aligned on top of the transparency. Place the other glass sheet/transparency assembly on top the PCB, very slowly and carefully, while observing proper alignment. Once alignment has been achieved, carefully, but firmly, hold both sheets together by the edges. Place a spring clip on each corner. After proper alignment has been confirmed by close observation, remove the piece of white paper and center the completed exposure assembly on the exposure platform. Turn on the PC557-F exposure lamp and expose the first side for ten minutes at a distance of six inches. Turn the board over and expose the other side for an additional ten minutes. Turn the PC557-F exposure lamp, remove the spring

clips and remove the exposed PCB by its edges. Proper safety equipment and procedures must be followed when handling sodium hydroxide and ferric chloride. Please refer to all cautions and instructions provided with these chemical products as well as the Material Safety Data Sheets (MSDS). The PCB is immersed in the developer solution for about two minutes while applying a gently agitation and observing the progress of the process. It may be necessary to remove the board from the developing solution for periodic inspection. After the PCB has been rinsed off and inspected, it may be returned to the solution for further developing or rinsed in cold water for an additional two to four minutes. The PCB is dried and inspected for flaw such as broken traces, defective pads, etc. If any flaws are found, the repairs may be made with an ink resist pen or resist patterns. In the case of using an ink resist pen, multiple applications may be required with at least two hours of drying time between applications or before etching. Again, following all safety procedures and using proper safety equipment, the developed PCB is immersed in a glass or plastic tray containing the ferric chloride etchant. The tray is gently agitated for one-half minute, than the PCB is removed and inspected. The unwanted copper of the PCB should have a much shinier appearance than what it was prior to immersion. If not, repeat the developing process for another one-half minute, rinse thoroughly, return the PCB to the etchant tray for one-half minute and inspect. Repeat developing process if necessary or return the PCB to the etchant tray until all the unwanted copper is dissolved. Rinse the board in cold running water for at least two minutes, then dry with paper towels. The PCB is ready for drilling. Start with a #70 drill (0.028 inch diameter) as a pilot for all pads with holes. Hole sizes are increased for certain parts and are redrilled accordingly. The parts are mounted and soldered onto the PCB with strict adherence to any keying or polarity markings on the parts placement illustration and the parts list.

It may be necessary to fabricate a glass exposure kit for one reason or another. For whatever the reason, the experimenter must be aware of the type of glass that is being substituted for the recommended kit. Commercial glass for windows is not acceptable for this exposure application because it does not transmit UV light lower than 400nm (4000Å). This type of glass is also known as float glass, plate glass and soda lime glass. Lead glass is also not suitable for this application. The glass must be able to transmit UV light in the range from 440nm (4400Å) to 350nm (3500Å). BK7 is a low dispersion borosilicate crown glass that has a transmission range of 350nm (3500Å) to 2000nm (20000Å). Optical grade fused silica has a transmission range of 260nm (2600Å) to 2500nm (25000Å). UV grade fused silica has a transmission ranges of 180nm (1800Å) to 2500nm (25000Å) and 300nm (3000Å) to 3700nm (37000Å). The three aforementioned types of glass are examples that are relatively common and suitable for this application. These examples will serve as a guide in making a purchase from a knowledgeable vendor. Make every effort to determine the type and the transmission range of the glass. The glass should be as thin as a common window, but not thinner. The two sheets of glass are cut to the appropriate size of six inches by nine inches with the corners as square as possible. The spring clips supplied with the recommended exposure kit may be replaced with paper binder clips available at most office supply stores.

SECTION TWO-VIDEO SYNCHRONIZATION

The color television standard currently in use in the United States of America is known as the NTSC or National Television Standard Committee color television system established in 1953. The ATSC or Advanced Television Systems Committee founded in 1982 establishes voluntary standards for DTV or Digital Television. While NTSC standards include those standards governing SDTV or standard definition television formats of various aspect ratios or screen formats, the ATSC DTV standards govern HDTV (High Definition Television) format and EDTV (Enhanced Definition Television) format as well as SDTV. The NTSC standard will be examined first with its European counterparts, the PAL (Phase Alternating Line) system and the SECAM (Sequential Color and Memory) system. A tutorial of the ATSC DTV standards confined only to analog HDTV will follow with reference to its European counterpart, the DVB (Digital Video Broadcasting) standard. Although analog HDTV signal processing is not directly applicable within the context of this project, this tutorial is presented in order to illustrate the complexity of and the variety of these video signals. It is with this tutorial and the content of this project that further experimentation with similar circuits to accommodate the processing of analog HDTV and other ASTC defined signals may be realized and is encouraged.

The NTSC standard, as well as the PAL and SECAM standards, require an encoding and decoding process. The result of the encoding process is a composite color video signal or CVBS signal. CVBS is the abbreviation for Composite Video Baseband Signal or Composite Video, Blanking, Synchronization. This encoding process combines the composite synchronizing signal, the monochrome luminance or Y signal and the color information. The video signal is a one volt p-p (peak to peak) signal which is divided into one hundred forty units known as IRE units. IRE is an acronym for Institute of Radio Engineers. These one hundred forty IRE units are calibrated into a scale from negative forty IRE units to positive one hundred IRE units, with zero as the blanking level of the signal. The region from zero to positive one hundred IRE units contains the video information to be viewed on the video display during the active video portion of a video line. The level of 100 IRE units is the peak white level. The region from zero to negative forty IRE units is normally reserved for the synchronizing pulses. The synchronizing pulses are the horizontal synchronizing pulse, equalizing pulses and the vertical serration pulses. The horizontal synchronizing pulse provides the timing reference for the start of each video line. The assembly of successive video lines into a vertical plane results in a still picture referred to as a field or frame. The equalizing pulses and vertical serration pulses provide the required timing to produce a repetition of the fields or frame to produce a moving picture. A field of "odd" numbered lines and a field of "even" numbered lines are required to produce a complete still picture or frame in the interlaced scanning format of video signal transmission. The NTSC standard has a total of 525 lines per frame with 480 active lines. This is known as 480i, with the "i" as a designation for interlaced scanning. Likewise, the PAL and SECAM standards have a total of 625 lines per frame with 576 active lines. This is known as 576i. Progressive scanning is just as the name implies, with all lines of a particular transmission being scanned in a sequential manner to produce an entire frame and

is classified as an EDTV format and has a designation "p". This format will be briefly reviewed latter in this text. In the subsequent text, all future reference will be in regard to the composite synchronizing signal or composite sync signal, which excludes any consideration of the video information contained in the active video portion of the video line.

Figure One A and Figure One B, accompanied with Table One, illustrates the typical horizontal synchronizing pulse interval and the composite synchronizing signal of one video line, respectively, of the NTSC, PAL and SECAM standards. The horizontal synchronizing pulse interval is more commonly known as the horizontal blanking interval or HBI. A comparison of the labeled components of the figures and their corresponding values in the table, indicate that the structure of the composite synchronizing signals of the three SDTV standards contain identical components, except for the color burst, differing only in time durations. Footnotes below the table define specific differences and similarities of the standards. One major difference between the standards is that the NTSC and the PAL standards each utilize a color burst of several cycles at a single specific frequency, with each standard having a different frequency, within the back porch interval. The SECAM standard uses a F_{OB}/F_{OR} burst also occurring during the back porch interval. The NTSC and the PAL standards each employ phase modulation (PM) techniques to transmit B-Y and R-Y difference signals. The B-Y and the R-Y difference signals are derived in the encoding circuitry from the blue or B component, the red or R component and the monochrome luminance or Y signal. The monochrome luminance or Y signal is a combination of mathematically proportioned gamma corrected blue, red and green components. This luminance or Y signal can produce a monochrome video display with a range from a black display to a white display. This method of producing only two difference signals enables the decoder to produce all three color components necessary for a color video display. Each difference signal is modulated on a chroma subcarrier of the same frequency with a ninety degree phase difference or "in quadrature". The color burst of the NTSC and the PAL standards provide a synchronizing signal for the local chroma subcarrier oscillator in the color decoder of the video processing device. The color burst of the NTSC standard is generated in the same phase in all successive lines, while the color burst of the PAL standard is generated in an alternating phase in each successive line. The SECAM standard uses frequency modulation (FM) to transmit B-Y and R-Y difference signals. Each difference signal has its own subcarrier defined as F_{OB} for the B-Y component and F_{OR} for the R-Y component. The F_{OB} subcarrier is assigned a frequency of 4.25 megahertz and the F_{OR} subcarrier is assigned a frequency of 4.40625 megahertz. Each of these FM subcarriers is transmitted on alternate scan lines sequentially. In order to identify and synchronize the line alternating sequence, a F_{OB} or a F_{OR} burst is generated during the back porch interval. The current burst then synchronizes the corresponding local chroma subcarrier oscillator of the two oscillators in the color decoder of the video processing device. Therefore, Table One has the designation of F_{OB}/F_{OR}* for the value of the color burst frequency in the SECAM column indicating reference to a footnote. In all standards these burst periods of oscillations are centered around the 0 IRE blanking level of the composite sync signal. This parameter must be properly

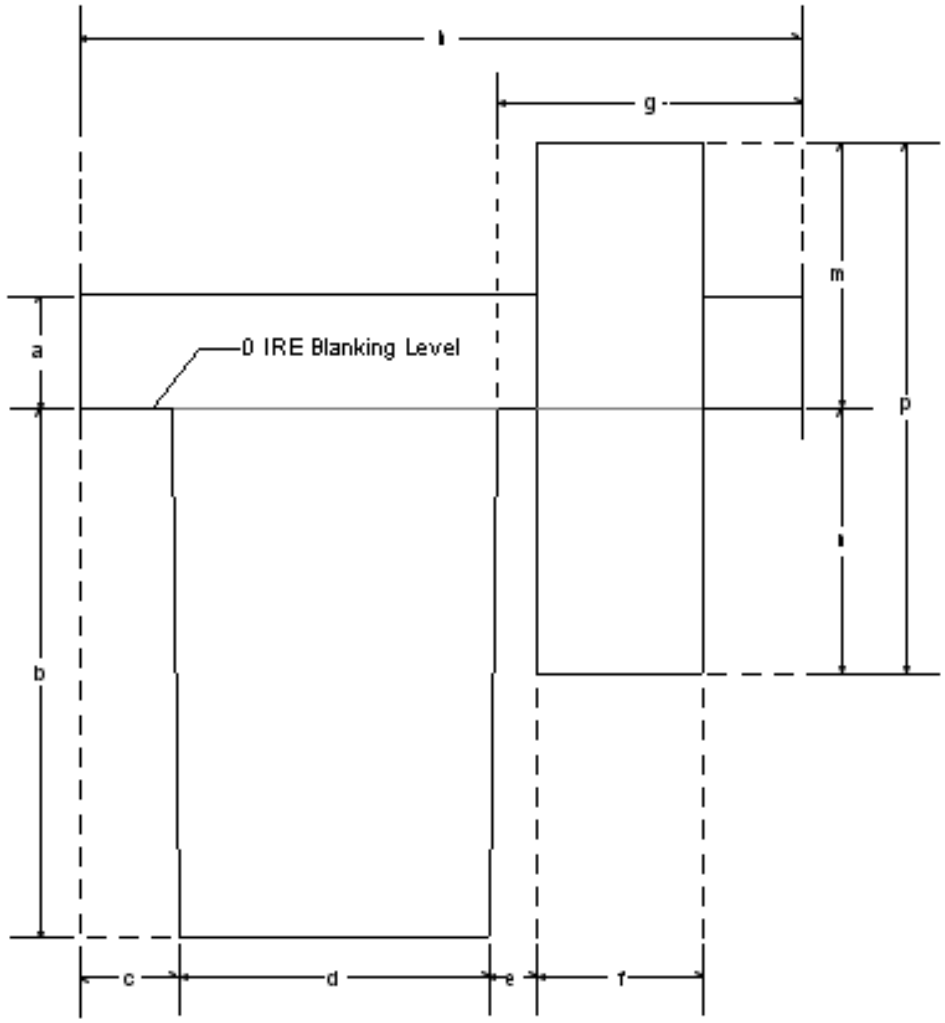


Figure One A

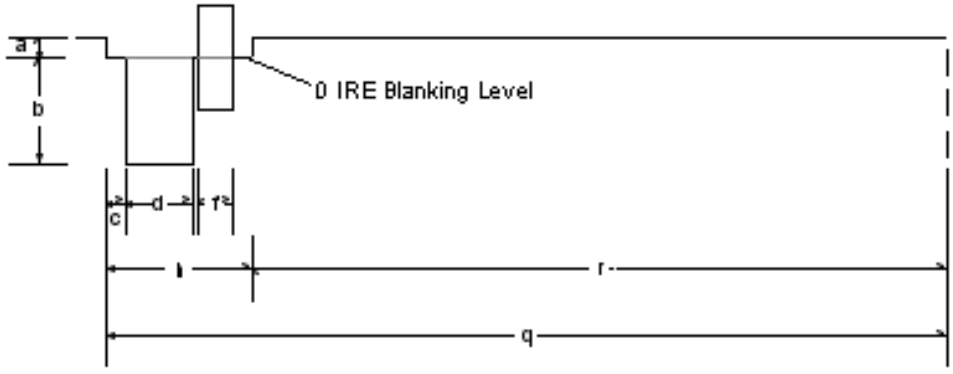


Figure One B

Dim.	Label	NTSC	PAL	SECAM	Units
–	Composite Video	1.0 V P-P	1.0 V P-P	1.0 V P-P	Peak-to-Peak Volts
–	Composite Video	140	143	143	IRE
–	Maximum Video Level	100	100	100	IRE
a	black level**	+7.5	–	–	IRE
b	horizontal sync magnitude	-40	-43	-43	IRE
c	front porch	1.5	1.5	1.65	microseconds (us)
d	horizontal sync duration	4.7	4.7	4.7	microseconds (us)
e	breezeway	0.6	0.9	–	microseconds (us)
f	color burst duration*	9±1	10±1	–	number of cycles
f	color burst frequency*	3.579545	4.43361875	F_{OB}/ F_{OR}	megahertz (MHz)
g	back porch	4.7	5.8	5.65	microseconds (us)
h	horizontal blanking interval	10.9	12.0	12.0	microseconds (us)
m	positive color burst magnitude	+20	+21.43	–	IRE
n	negative color burst magnitude	-20	-21.43	–	IRE
p	total color burst magnitude	40	42.86	–	IRE
q	complete video line	63.55558	64.0	64.0	microseconds (us)
r	active video region	52.65558	52.0	52.0	microseconds (us)

Footnotes:

* F_{OB} : FM subcarrier for B-Y difference signal equal to 4.25 megahertz
F_{OR} : FM subcarrier for R-Y difference signal equal to 4.40625 megahertz

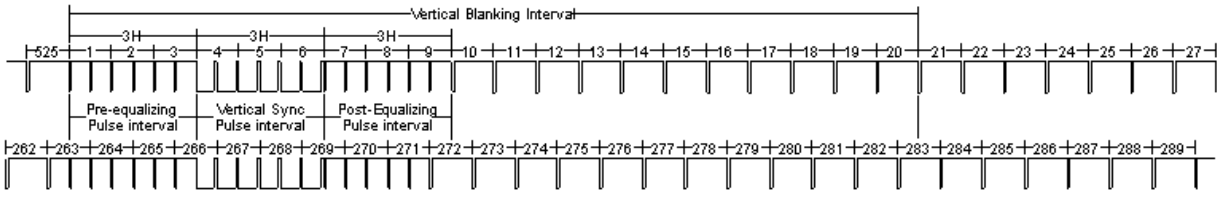
** The black level or blanking pedestal is used only in the NTSC standard for set-up

Table One

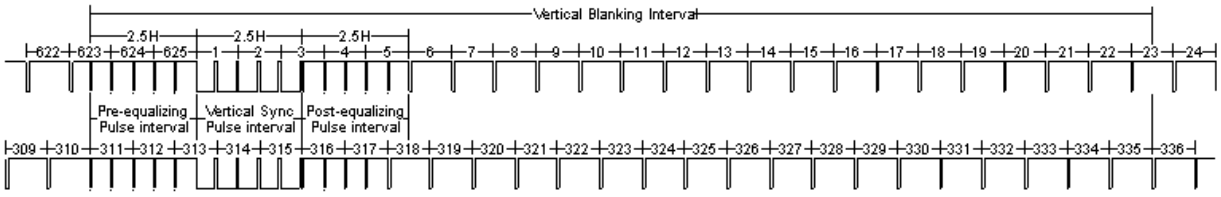
maintained in all standards for proper color decoding. As Figure One and Figure Two illustrate the front porch and the back porch are maintained the 0 IRE blanking level. It is this 0 IRE blanking level which provides a reference level for each line. This reference level also occurs in the vertical blanking interval of the composite sync signal. These levels are maintained in this project by the implementation of the ISL4089 DC restoration IC as will be demonstrated in Section Three of this manual. A subtle difference between the NTSC standard and the PAL and SECAM standards, is that the NTSC standard uses a set-up or reference black level of 7.5 IRE.

Figure Two, accompanied with Table Two, illustrates and defines the vertical blanking interval (VBI) of the interlaced scanning formats of the NTSC and of the PAL and SECAM standards. Each set of illustrations are in a relatively accurate approximate scale to one another. The lines of each set are numbered in accordance to accepted convention of each standard's definitions and designations.

It should also be noted that each set of figures has an even field and an odd field. These figures are a general representation of the several formats currently in use, but are more than adequate for application to this project. Upon comparison of the two sets of figures, the vertical blanking intervals have the same major components and partitions. Each corresponding partition differs only in the quantity of the types of components or pulses and the time allotment. These similarities are prevalent throughout all formats of all the NTSC, PAL and SECAM standards. The partitions of Figure Two are the pre-equalizing pulses, the vertical synchronizing pulses and the post-equalizing pulses. The descriptions of these partitions are further enhanced by the numerical data supplied in Table Two. The vertical synchronizing pulses are preceded by the pre-equalizing pulses and are followed by the post-equalizing pulses. Both sets of equalizing pulses are twice the horizontal line scan frequency or line frequency and serve to minimize the effect of the line frequency pulses on the processing of the vertical synchronizing pulses. The vertical synchronizing pulses are processed by an integration circuit to create a vertical sync signal that is recognized by the video processing device and make each vertical deflection start at the correct instant for proper interlace.



NTSC VBI



PAL and SECAM VBI

FIGURE TWO

The remaining blanked lines of the vertical blanking interval immediately following the post-equalizing pulses are the top of the raster and the start of the downward vertical trace. These lines are regulated by the FCC and include special communication and reference signals or VBI data. It is a common practice to insert the VBI data in up to five scan lines of the active picture region of the raster. This is to ensure that specific data from broadcasters wouldn't be inadvertently altered or eliminated due to video signal processing by the cable companies and other

Parameter	NTSC	PAL/SECAM	Units
Equalizing/Vertical Partition*	3.0	2.5	Lines
Equalizing/Vertical Partition*	190.667	160.00	Lines
Equalizing/Vertical Period**	0.5	0.5	Lines
Equalizing/Vertical Period**	31.778	32.000	Microseconds
Equalizing Pulse	2.3	2.35	Microseconds
Equalizing Serration	29.478	29.65	Microseconds
Vertical Sync Pulse	27.278	27.3	Microseconds
Vertical Sync Serration	4.5	4.7	Microseconds
No. of Pulses per Partition	6	5	Pulses
VBI Blanked Lines per Field	11	12.5	Lines
VBI Duration	20	25	Lines
VBI Duration	16.6833	20.00	Milliseconds
Active Lines per Field	242.5	288	Lines
Active Lines per Frame	485	576	Lines
Lines per Field	262.5	312.5	Lines
Lines per Frame	525	625	Lines
Field Frequency	59.94(60/1.001)	50	Fields/Second
Frame Frequency	29.97(30/1.001)	25	Frames/Second
Horizontal Scan Frequency	15,734.26	15,625.00	Lines/Second
Horizontal Line Duration	63.55558	64.00000	Microseconds
Closed Captioning Placement***	21 & 284	22 & 335	Line Lumber
Longitudinal Timecode Start	5±1.5	2±1.5	Line Number
Vertical Interval Timecode Placement	14 & 277	19 & 332	Line Number
Widescreen Signaling Placement	20 & 283	23	Line Number

* Each Partition: Pre-equalizing Pulse Partition, Vertical Sync Pulse Partition and Post-equalizing Pulse Partition

** Start of pulse to start of next pulse

*** May occur between lines 21 thru 25 inclusive and lines 284 thru 289 inclusive for NTSC or between lines 22 thru 26 inclusive and lines 335 and 339 inclusive for PAL/SECAM.

TABLE TWO

sources. The effects of this practice remain unnoticed because it is masked by the video display device's overscan. The types of VBI data which are inserted are closed captioning, teletext, time code and widescreen signaling. Each of these types of VBI data are assigned specific blanked lines to be inserted into. Table Two

lists these types of VBI data and the lines that they are assigned to, of the most common formats of the NTSC, PAL and SECAM formats used. This project involves the DC restoration to ground of potions of most of the blanked lines of the vertical blanking interval. Some, if not all, of the VBI data must be considered in the application of this project depending upon the experimenter's analysis criteria. Blanked video lines containing VBI data may be allowed to pass unaltered if allowed to do so by the user program. Methods of programming the microcontroller to perform these exceptions will be examined in Section Three, Subsection C. The VBI data which must be considered includes closed captioning (EIA-608) and wide screen signaling (WSS). These two types of VBI data are of the most concern to the average individual viewing any video program. Closed captioning is a service which requires a decoder to display text at the bottom of the video display. This service is generally used to insert subtitles for the hearing impaired. In the NTSC standard, the EIA-608 specification regulates the usage of this service. In the ATSC standard the EIA-708 specification regulates the usage of this service. EIA-608 specifies that the closed captioning data appear on lines 21 and 284 of an interlaced display, but occasionally may appear on any line between 21-25 and 284-289. For (M) PAL, closed captioning data appears on lines 22 and 281, but may occasionally appear on any line between 18-22 and 281-285. For (B, D, G, H, I N, NC) PAL video media, closed captioning data appears on lines 22 and 335, but occasionally appear on any line between 22-26 and 335-339. In the NTSC and PAL standards, the data format, amplitudes, and rise and fall times are identical, with exception the timing due to the difference in line frequency. The other standards in other countries regulate closed captioning in their own manner. There are not any international standards governing or regulating the usage of closed captioning. Widescreen Signaling (WSS) is incorporated by NTSC, PAL and SECAM standards as a means to direct widescreen video display devices to display the correct aspect ratio of the video signal being received. WSS data is transmitted on lines 20 and 283 of the interlaced 525-Line NTSC standard. WSS data is transmitted on line 23 of the interlaced 625-Line PAL and SECAM standards. WSS data also appears on line 41 of the 480p formats and on line 43 of the 576p formats of the EDTV formats. Time codes are generally used to assist in the editing of recorded video material. Two types of time codes, for encoding time for video or audio in hours, minutes, seconds and frames, are commonly used. These are known as longitudinal timecode (LTC) and vertical interval timecode (VITC). Both codes contain the time data on a BCD system. The LTC code begins at line 5±1.5 lines for the 525-line systems, at line 2±1.5 lines for the 625-line systems and at the vertical sync timing reference of the frame ±1 line for the 1125-line systems. This LTC word is evenly spaced throughout the remainder of the entire frame. The VITC time code is serial data and appears on lines 19 and 332 (or 21 and 334) for the 625-line (576i) systems, lines 14 and 277 for the 525-line (480i) systems and lines 9 and 571 for the 1125-line (1080i) SYSTEMS. Teletext is a method of transmitting data within a video signal. There are seven teletext systems currently in use with one, System B, being the most internationally used. System B is also known as "World System Teletext" or WST. The information is transmitted in the form of pulse-code modulation (PCM) signals normally using two unused lines of the VBI although data ay be transmitted on any line. The data rate

for teletext for approaches 7 Mbps, which greatly exceeds that of closed captioning. Teletext may be displayed as pages of text, on a display device, which requires special equipment for decoding and utilizing the signals. In some cases, teletext is used to insert subtitles for people with impaired hearing and therefore may be compensated for at the experimenter's discretion.

The final topic of the ATSC standard will consist of brief discussions of each analog EDTV formats and analog HDTV formats. Most analog EDTV and analog HDTV systems incorporate analog YR'G'B' signals or YPbPr signals. Using analog YR'G'B' or YPbPr video signals eliminate NTSC/PAL encoding and decoding circuitry, and the associated intermediate carrier and sub carrier signals. This results in greater clarity of the video display with less noise from the less than perfect removal of carrier signals. The use of YR'G'B' and YPbPr signal interfaces are not confined to HDTV, but available for all analog video signal processing devices. Each analog interface have digital counterparts, namely DVI (Digital Visual Interface) or digital RGB, which is analogous to analog YR'G'B' and HDMI (High Definition Multimedia Interface) or digital YCbCr, which is analogous to analog YPbPr. In the case of the analog YR'G'B' signal interface, the R' signal is the gamma corrected red video signal or channel, the G' signal is the gamma corrected green video signal or channel, and the B' signal is the gamma corrected blue video signal or channel. Gamma correction is the modification of the linearity of the amplitude of a video signal to compensate for the non-linear characteristics of display devices and the sensitivities of the human eye. Sync information is usually present on the green channel for the consumer market and present on all three channels for the pro-video market. In some cases, a separate composite sync signal or separate horizontal and vertical signals are supplied as additional channels. Examination of the YPbPr signal interface reveals that a Y channel, A Pb channel and a Pr channel constitutes the inputs. The Y channel is the video input for the luminance or black and white component combined with the composite sync signal. The Pb channel is the B-Y difference signal as described earlier in this text. Likewise, the Pr channel is the R-Y difference signal as also described earlier in this text. The sync signal is present only in the Y channel of consumer market devices, but is present in all the channels for pro-video market devices.

The composite sync is a -40 IRE pulse for the analog EDTV formats. In the case of analog HDTV, the composite sync signal is a ±300 mV tri-level signal. Figures 3A and 3B, accompanied with Table Three, illustrates a typical analog EDTV horizontal blanking interval and a typical analog HDTV horizontal blanking interval, respectively, that may be referenced to while reviewing the following description of the most popular analog EDTV and analog HDTV signal formats. Each figure depicts the synchronizing pulse waveforms only and each are in an approximate scale, but not to each other. Table Three only lists the data for the YR'G'B' signal interface components, but not the YPbPr signal interface components. Analog EDTV video signals of 480p and 576p, each applicable to 4:3 and 16:9 aspect ratios, respectively, are defined by ITU BT.1358. Analog HDTV video signals of 720p, 1080i and 1080p are defined by ITU BT.709. ITU is the International Telecommunications Union, which replaced the CCIR or Consultative Committee in International Radio, is an international broadcast standards committee for

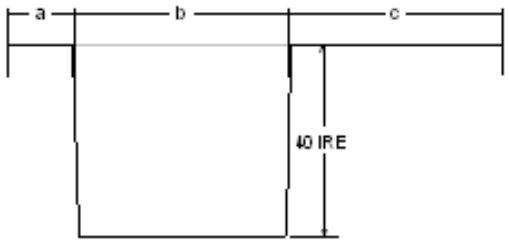


Figure 3A-EDTV

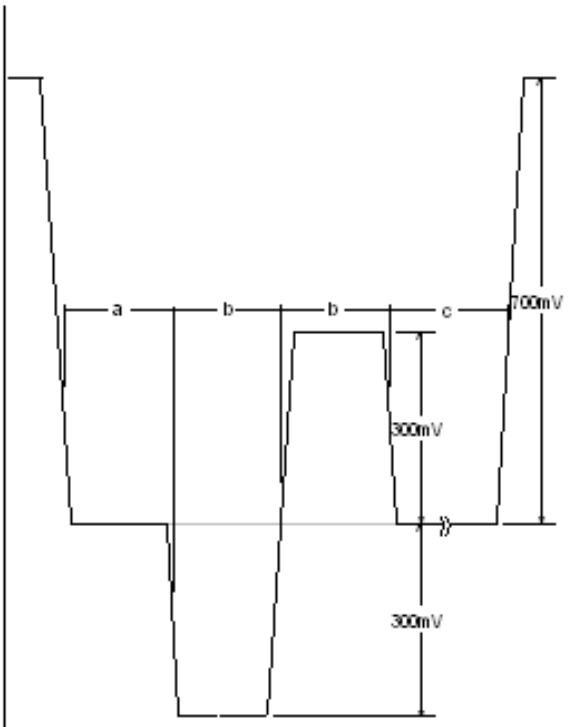


Figure 3B-HDTV

EDTV					
Resolution	720x480p	960x480p	720x576p	960x576p	
Actual	858x525	1144x525	864x625	1152x625	
Ratio	4:3	16:9	4:3	16:9	
Refresh Rate	59.94(60/1.001)	59.94(60/1.001)	50.00	50.00	
Sample Clk	27.000 MHz	36.000 MHz	27.000 MHz	36.000 MHz	
Line(us)	31.778	31.778	32.000	32.000	
HBI	138/5.111	184/5.111	144/5.333	192/5.333	Samples/Time(us)
Front Porch-(a)	16/0.5926	21.5/0.5972	84/2.33	78.5/2.18	Samples/Time(us)
Pulses-(b)*	63/2.33	12/0.4444	63/2.33	69/2.555	Samples/Time(us)
Back Porch-(c)	59/2.18	16/0.4444	84/2.33	92/2.555	Samples/Time(us)
HDTV					
Resolution	1280x720p	1920x1080i	1920x1080i	1920x1080p	1920x1080p
Actual	1650x750	2640x1125	2200x1125	2640x1125	2200x1125
Aspect Ratio	16:9	16:9	16:9	16:9	16:9
Refresh Rate	59.94(60/1.001)	25.00	59.94(60/1.001)	50.00	29.97(30/1.001)
Sample Clk	74.176 MHz	74.250 MHz	74.176 MHz	148.500 MHz	148.352 MHz
Line(us)	22.24	35.56	29.66	17.78	14.83
HBI	370/4.988	720/9.697	280/3.775	720/4.848	280/1.887
Front Porch-(a)	70/0.9437	484/6.52	44/0.5932	484/3.26	44/0.2966
Pulses-(b)*	40/0.5393	44/0.5923	44/0.5932	44/0.2963	44/0.2966
Back Porch-(c)	220/2.966	148/1.99	148/1.995	148/0.9966	148/0.9976

* The single pulse of the EDTV format and each pulse of the HDTV format

Table Three

telecommunications. The basic formats for analog EDTV of 4:3 and 16:9 aspect ratios are 720x480p and 960x576p, respectively. These two basic formats are predicated upon the values of 480 and 576 referring to the active lines without the VBI. There are 525 total lines for the 480p format and 625 total lines for the 576p format. Similarly, the values of 720 and 960 refer to the active portion or the active samples without the HBI. There are a different number of active samples for each variation of the extended formats, dependent upon the aspect ratio and the frame or refresh rate of the format being considered. The product of the frame rate, the total lines and the total samples yields the sample clock frequency. The frame rate also dictates the horizontal line scan duration and the horizontal blanking interval duration. For the EDTV formats cited in Table Three, there are two frame rates listed. The 480p formats have a frame rate of 59.94 (60/1.001) Hz with a horizontal line scan time of 31.776 microseconds. The 576p formats have a frame rate of 50 Hz with a horizontal line scan time of 32.000 microseconds. The frame rate does not although affect the horizontal sync pulse of any of the analog EDTV formats, which is 2.33 microseconds for all four derived formats.

Since the aspect ratios of analog HDTV displays are 16:9 in the United States, the basic formats are 1280x720p, 1920x1080i and 1920x1080p. These basic formats are predicated upon the values of 720 and 1080 referring to the active lines without the VBI. There are 750 total lines for the 720p format and 1125 total lines for both 1080i and 1080p formats. Similarly, the values of 1280 and 1920 refer to the active portion of a line or the active samples without the HBI. There are 1650 total samples for the 1280 active samples which relates to the 720p format. There are 2200 total samples or 2640 total samples for the 1920 active samples which relate to the 1080i and the1080p formats. The numbers of these total samples is dependent upon the frame or refresh rates. The product of the frame rate, the total lines and the total samples again yields the sample clock. The 720p format frame rate is usually 59.94 (60/1.001) Hz with a horizontal line scan time of 22.24 microseconds and a horizontal blanking interval of 1.887 microseconds. The 1080i format frame rates are usually 25 or 29.97 (30/1.001) Hz. The 1080i format with a frame rate of 25 Hz has a horizontal line scan time of 35.56 microseconds with a horizontal blanking interval of 9.697 microseconds. The 1080i format with a frame rate of 29.97 (30/1.001) Hz has a horizontal line scan time of 29.66 microseconds with a horizontal blanking interval of 3.775 microseconds. The 1080p format frame rates are usually 50 or 59.94 (60/1.001) Hz. The 1080p format with a frame rate of 50Hz has a horizontal line scan time of 17.78 microseconds with a horizontal blanking interval of 4.848 microseconds. The 1080p format with a frame rate of 59.94 (60/1.001) Hz has a horizontal line scan time of 14.83 microseconds with a horizontal blanking interval of 1.887 microseconds. It should also noted at this time, that in all cases, each horizontal sync pulse excursion is much less than one microsecond. It is because of this parameter that a tolerance of five nanoseconds must be observed for proper signal processing. This is the major limiting factor for the application of this project, with the currently available microcontroller(s), for use on HDTV formats. This concludes this video synchronization tutorial.

SECTION THREE-PROJECT ANALYSIS AND EVALUATION

Subsection A: Theory of Operation

As previously stated in this text, the test points will be assigned to the project circuitry during this discussion of operational theory. There are twenty test points labeled as TP1 through TP20 and shall be referred to as such for the remainder of this text. These test points are on the circuit board as two adjacent pads that are to have a wire, with each end soldered to a pad, forming a small loop. These loops will accommodate DVM and oscilloscope test hooks. It must be understood by the experimenter, that the text describes the suggested mode of operation of the project with the programs provided with the project. Minor changes in the program may result in varying degrees of operation and performance. Upon completion of initial programming and testing after assembly, the experimenter is encouraged to make minor and/or major changes in the program and observe the effects on a video display, as well as the test instrument displays. The basic version will be examined first. The advanced version is an extension of the basic version and will be examined in that context. As this discussion progresses, references will be made to the preliminary data sheets of the particular device and relevant circuitry being examined. These preliminary data sheets are included in the project package for the exception of the data sheets for the Atmel® microcontrollers. However, a pin-out diagram, prepared by J.L.K. Electronics, has been provided. This diagram is on page _ and designated as Figure Five. Complete data sheets for all IC devices are available on-line or direct contact from the manufacturers contained in the manufacturer listing. References will be made to the optional replacement devices listed for clarity and ease of substitution when appropriate.

The signal path begins at the video input and is thus labeled TP1. The video input is routed into three devices: IC1, the reference generator for the microcontroller; IC5, the inserter/stripper buffer amplifier and; IC6, the hybrid sync separator. IC1 is a LM1881 commercially available sync separator with a composite sync output, burst/back porch output, even/odd field output and vertical sync output. The replacement device, EL4581, has the same outputs and pin configuration as the LM1881. As this text progresses, the similarities as well as the differences and compensation for the differences of the EL1883 and ISL59885 replacement devices briefly described on page 3 in Section One, will be examined. Each output of the reference generator is connected to a separate pin in Port D of the ATtiny2313V microcontroller designated as IC2. The vertical sync output, pin 3 of IC1, is connected to pin 7 of IC2 and is labeled TP2. This pin is referred to as PD3 and is configured as Interrupt 1 or INT1. Upon receiving a vertical sync pulse the main program begins. This is known as an interrupt-generated program. At the beginning of the program, the status of TP5 is tested to confirm if the ISL59885 is currently in use. A low input would indicate its presence in the circuit and an HDTV video signal input is being received. The program would be terminated and the signal would be allowed to pass unaltered. A high input would be inconclusive as to which reference generator is being used but would be a strong indication that the video signal being received is a SDTV video signal. Since this project is not intended for HDTV video signal processing, it is assumed that the experimenter will apply a HDTV signal for

experimental observations only. The next test is the status of the AuxIn terminal of the basic version. This input terminal is pulled high by an internal pull-up resistor in the program and is connected to an optional switch to ground. If there is no switch employed or the switch is open, the program is directed to the NTSC subroutines. If there is a closed switch to ground employed in the circuit, the program is directed to the PAL/SECAM subroutines. In the case of the advanced version, the program of the ATtiny13 auxiliary microcontroller is specifically written for the purpose of identifying which format grouping is currently being processed. There are two groups of formats to be processed, with the NTSC format comprising one group and the PAL format with the SECAM format comprising the other group. The program for the auxiliary microcontroller distinguishes between the two format groupings on the basis of field duration difference. It may also be possible for the experimenter to modify a portion of the program of the auxiliary microcontroller to detect the difference between the vertical pulse durations of the two format groupings. This concept is of presented as exercise number five in subsection C for the experimenter to explore. IC2 then spontaneously generates the remainder of the vertical sync pulses and the post-equalizing pulses as programmed for the detected format grouping. It is during the processing of the last post-equalizing pulse that the status of TP4 is examined. TP4 is the test point of the even/odd output field output, pin 7, of IC1 which is connected to pin 9 or PD5 of IC2. The status of TP4 dictates whether the even subroutine or the odd subroutine of the detected format is selected. The EL1883 and the ISL59885 do not have an even/odd field, but have a horizontal output instead. Use of these devices in both versions will identify the current field being processed because of the placement of the status test in the program and the timing output of the EL1883 and the ISL59885. IC2 then responds to each horizontal sync pulse of the composite sync output, pin 1 of IC1 which is connected to pin 8 or PD4 of IC2 and is labeled TP3. The program then generates the appropriate pulses at the outputs of IC2 until the end and then awaits another interrupt and the process repeats or loops. The Port B pins of IC2 are designated as outputs.

IC6, the hybrid sync separator, is designed around the OPA698 voltage limiting operational amplifier which is configured as an open-loop comparator. The circuit operation is dependent upon the biasing of pin 5, the low voltage limiting pin or V_L and pin 8, the high voltage limiting pin or V_H, as well as pin 2, the inverting input and pin 3, non-inverting input. The proper biasing of these pins will enable IC6 used to detect extraneous and spurious signals as well as the horizontal sync pluses and possibly color burst. Pin 5, the low voltage limiting pin or V_L, is biased at ground and pin 8, the high voltage limiting pin or V_H, is biased at V_{cc} or 5.0 volts. The video input signal is applied to pin 3, the non-inverting input and pin 2, the inverting input, is biased at negative 0.204 volt or approximately negative 28.5 IRE. Any pulses or signal below the threshold of negative 28.5 IRE will appear at pin 6, the output of IC6, as ground and any pulses or signal above this threshold will be at V_{cc} or 5.0 volts. The output is therefore determined by the voltage limiting pins and not by any default level. The output, pin 6 of IC6, is connected to pins 4 and 5 of IC7a and is labeled as TP6. IC7 is a CD4023, triple 3-input NAND gate. The output, pin 6 of IC7a, is connected to pins 1, 2 and 8 of IC7b, effectively making the combination of gate IC7a and gate IC7b an AND gate. The last input, pin 3 of IC7a, is connected to

pin14 or PB2 of IC2 and labeled as TP7. The output, PB2 of IC2, is programmed as a horizontal sync pulse source and goes from "high" to "low" when PD4 detects a horizontal sync pulse from IC1. This output is logically combined with the output of the hybrid sync separator and programmed to ensure a proper horizontal sync pulse length of 4.7 microseconds. Upon completion of the horizontal sync pulse source timing, the program instructs the output, PB2 of IC2, to go from "low" to "high". The output, pin 9 of IC7b, is connected to pin 12 of IC8d and is labeled as TP8. IC8 is a CD4001, quadruple 2-input NOR gate or a CD4071, quadruple 2-input AND gate. The output, pin 11 of IC8d, is connected to pins 8 and 9 of IC8c, effectively making the combination of gate IC8c and gate IC8d an OR gate. The last input, pin 13 of IC8d, is connected to pin 16 or PB4 of IC2 and labeled as TP9. The output, PB4, is programmed as a breezeway/burst pulse source and goes from "low" to "high" during the same instruction that concludes the horizontal sync pulse source timing of PD2. This output is logically combined with the output of IC7b, to ensure that durations of the breezeway and the burst of the back porch region are not altered during further processing. The output, pin 10 of IC8c, is connected to pin 2 of IC8a and to pin 6 of IC3b and pin 8 of IC3c and is labeled TP10. The signal at TP10 has a corrected horizontal sync pulse, compensated breezeway/burst region with any other extraneous and spurious signals. The output, pin 3 of IC8a, is connected to pins 5 and 6 of IC8b, effectively making the combination of gate IC8a and gate IC8b an OR gate. The last input, pin 1 of IC8a, is connected to pin 15 or PB3 of IC2 and labeled as TP11. The output, PB3, is programmed as a pulse-to-pulse interval source and also goes from "low" to "high" during the same instruction that concludes the horizontal sync pulse source timing. This output is logically combined with the output of IC8c, to produce a completely corrected sync signal less the extraneous and spurious signals that is synchronized with the incoming video signal. The output, pin 4 of IC8b, is connected to pins 11, 12 and 13 of IC7c, pin 1 of IC3a, pin 5 of IC3b and pin 11 or PD6 of IC2 and is labeled TP 12. The signal at TP12 is the corrected composite sync signal. The output, pin 10 of IC7c, is an inverted output of IC8b, to be inserted into the video signal and is labeled as TP13. The IC3 is a CD4011, quadruple 2-input NAND gate which is hardwired to function as an exclusive OR gate. One input of this exclusive OR gate consists of pin 6 of IC3b and pin 8 of IC3c. As previously stated, this input is connected to the output of IC8c. The other input of this exclusive OR gate consists of pin 1 of IC3a and pin 5 of IC3b. As previously stated, this input is connected to the output of IC8b. The output of this hardwired exclusive OR gate is pin 11 of IC3 and produces an error signal consisting of the extraneous and spurious signals to be removed or stripped from the video signal and is labeled TP14.

The inverted corrected composite sync signal at TP13 is connected to the inverting input, pin 2, of IC9. IC9 is an OPA698 voltage limiting operational amplifier which is configured as an open-loop comparator to function as a digital-to-analog converter or DAC. This analog voltage will be inserted into the video input signal via pin 8, the high voltage limiting pin or V_H, of the inserter/stripper buffer amplifier, IC5. IC5 is an OPA698 voltage limiting operational amplifier which is configured to function as an amplifier having a gain of two with voltage limiting capabilities. Pin 5, the low voltage limiting pin or V_L, of IC9 is biased at negative 0.575 volt or

approximately negative 80.5 IRE and pin 8, the high voltage limiting pin or V_H, is open. Pin 3, the non-inverting input of IC9, is biased at positive 2.5 volts. When the input at pin 2 falls below the threshold of 2.5 volts, the voltage at pin 6, the output of IC9, be limited to a negative 0.575 volts. This value is twice the normal negative 40 IRE of the composite sync signal because the gain of the inserter/stripper buffer amplifier, IC5 is two. The inverted corrected composite sync signal is inserted into the inserter/stripper buffer amplifier, IC5, via pin 8, the high voltage limiting pin or V_H, of IC5. When the input at pin 2 rises above the threshold of 2.5 volts, the voltage at pin 6, the output of IC9, is allowed to pass unaltered because pin 8, the high voltage limiting pin, is open and therefore unbiased. This has the same effect on pin 8, the high voltage limiting pin or V_H, of IC5 by allowing the video signal to pass unaltered, except for the amplification by a factor of two. The output, pin 6 of IC9, is labeled as TP15.

The error signal consisting of extraneous and spurious signals at TP14 is connected to the non-inverting input, pin 3, of IC4. IC4 is an OPA698 voltage limiting operational amplifier which is configured as an open-loop comparator to function as a DC restoration to ground switch. The switch to ground is activated upon receiving an error signal. This inserts a ground signal into the video input signal and effectively strips the error signal from the video input signal, via pin 5, the low voltage limiting pin or V_L, of the inserter/stripper buffer amplifier, IC5. Pin 5, the low voltage limiting pin or V_L, of IC4 is open and therefore unbiased and pin 8, the high voltage limiting pin or V_H, is connected to ground. Pin 2, the inverting input of IC4, is biased at 2.5 volts. Pin 6, the output of IC4 is connected to pin 5, the low voltage limiting pin or V_L, of IC5. When there are no error signals, the signal voltage remains at zero and thus below the threshold of 2.5 volts. Since pin 5, the low voltage limiting pin or V_L, of IC4 is open, the output at pin 6 of IC4 passes this open effect to pin 5, the low voltage limiting pin or V_L, of IC5. Under these conditions, the video signal passes through IC5 unaltered, except for the amplification by a factor of two. When an error signal is present and exceeds the threshold of 2.5 volts, the output at pin 6 of IC4 shifts to ground due to pin 8, the high voltage limiting pin or V_H, of IC4 being connected to ground. This effect is passed to pin 5 of IC5, and the output at pin 6 of IC5 is grounded in accordance to the error signal. This action eliminates or strips the error signal from the video input signal. Pin 6, the output of IC4 is labeled TP16. The output at pin 6 of IC5 is the sync corrected video signal and is labeled TP17.

The sync corrected video signal at TP17 is connected to the non-inverting input, pin 2, of IC10. IC10 is an ISL4089 DC restored video amplifier which is configured for a gain of two. Pin 3 of IC10 is the voltage reference pin or V_{REF} to which the correction voltage that the video signal is be DC restored is applied. Pin 4 of IC10 is the HOLD pin or the switching control which activates the DC restore function. The HOLD pin is a logic input with a logic "low" being the active state of the pin and the correction voltage at pin 3 of IC10 is applied to the video signal. For correction voltages other than ground, the output will be DC restored or clamped to the resultant voltage of the product of the corrective voltage and the gain of the ISL4089. Pin 3 of IC10 is connected to a dual adjustable voltage divider network. Each branch is connected to a separate output pin of the microcontroller, IC2. Pin

18, or PB6, of IC2 is one branch and pin 19, or PB7 of IC2 is the other branch. Only one pin is active at any one time and is determined by the program. These two user determined voltages, in addition to the ground state when both outputs are not active, are meant to provide the experimenter with optional avenues for experimentation. In the supplied program, both outputs are inactive and therefore at ground. As a result the V_{REF} pin, pin 3 0f IC10, is at ground potential and labeled as TP18. The HOLD pin, pin 4 of IC10, is connected to pin 17, or PB5, of IC2 and is labeled as TP19. The supplied program begins the activation sequence of the HOLD pin immediately after the first post equalizing pulse and only deactivates during the remaining post equalizing pulses and the horizontal sync pulses of the blanked video lines of the vertical blanking interval or VBI. The HOLD pin is only active during the back porch of each of the remaining active lines of the field being processed. The output, pin 7 of IC10, is the AGC/sync corrected video signal and labeled as TP20. This concludes the basic version theory of operation portion of this text.

The advanced version differs from the basic version in the addition of an auxiliary microcontroller, IC2A. IC2A is an ATtiny13 microcontroller which has the purpose identifying which reference generator, IC1, is in use. and if necessary, implementing the subroutine of the program to compensate for the inherent difference. The inherent difference is that the EL1883 and the ISL59885 each lack an even/odd field output. Pin 2 of IC2A is the clock input and is connected to the clock out, pin 6 or PD2, of IC2. All outputs of the reference generator are each connected to an input of IC2 and an input of IC2A. Pin 3 or PB4 of IC2A is configured as an output to input, pin 3 or PD1, of IC2. This output will be the auxiliary even/odd field detection port. This port will also serve as a high definition signal detection port in the case of the ISL59885 and as will be seen in the next subsection, the program will direct the regulator to pass the signal unaltered.

Subsection B: Program Description

The program for the basic version and the advanced version of IC2, the ATtiny2313, are the same. The program is known as an interrupt-generated program. The interrupt is generated every field by the vertical sync pulse at pin 7, or PD3, of IC2 which is configured as INT1 or Interrupt 1. The interrupt INT1 vector and the reset vector are in the first section of the program below the title box with the comment, "Interrupt service vectors". This is known as the "Program memory vector table" which is the lowest part of the AVR program memory, starting at address $0000. The .org directive is used to set vector jump locations. At address $0000, the Reset vector is the address for the "RESET" label or block of code in the third section of the program. This block of code "handles" the stack pointer set up, the Data Direction Registers, initial output state, internal pull-up resistor activation and the interrupt mask. Once the "sei" or the "set global interrupt flag" instruction has been executed, the program then moves to the "LOOP" label which is followed by a jump instruction to the "LOOP" label. The program then loops until an interrupt INT1 occurs. The .org INTIaddr directive sets the vector jump to the "INTV1" label in the fourth section of the program.

The fourth section, INTV1, is the final part of the "common" program. The

detection of a SDTV video signal or a HDTV video signal, the selection of the NTSC format subroutine or the PAL/SECAM format subroutine and the selection of the even field subroutine or the odd field subroutine of the appropriate format is done in this fourth section. The operation of these decision processes were briefly examined in the previous subsection. It is also in the fourth section that the microcontroller begins the generation of horizontal sync pulse partitions, breezeway/burst pulse partitions, pulse-to-pulse interval partitions, DC restoration voltage selection and DC restoration voltage control. Another function of this section is to spontaneously generate the remainder of the vertical sync pulses and the post-equalizing pulses to precisely coincide with their VBI counterparts. It is now that the "declarations" of the second section of the program become an integral part of the program. These "declarations" define the temporary registers r16, r17, r18 and r19. Each register is assigned a specific type of value with its own numerical representation in order to readily distinguish itself from other values with the content of the program. Register r16, temp, is reserved for the outputs of the microcontroller and is expressed in binary notation. Register r17, temp1, is reserved for the amount of lines and pulses of the composite sync signal and is expressed in decimal notation. Register r18, temp2, is reserved for time or duration of pulses to be counted down and is expressed in hexadecimal notation. Register r19, temp3, is reserved for the additional amount of lines of the PAL/SECAM standards contain. The total amount of lines of the PAL/SECAM standards cannot be stored in a single register, because the amount exceeds its one byte capacity of 255, $FF or 0b11111111. Each of the temporary registers is repetitively decremented and tested in order to branch to other labels within the program. This method of decrementing and testing registers provides an accurate source of counting pulses and timing the duration pulses by counting the cycle times of the ATtiny2313. Most of the instructions of the ATtiny2313 use only one machine cycle per instruction. Since the clock frequency of the ATtiny2313 is twenty megahertz, a machine cycle has duration of fifty nanoseconds. A "dec" instruction with a "brne" instruction uses three machine cycles, or one hundred fifty nanoseconds, if the "brne" is true. If the "brne" is false, this combination uses two machine cycles or one hundred nanoseconds. If "nop", or no operation, instructions are added to the loop, fifty nanoseconds are added for each instruction. This "counting down' technique also allows for other tests to be performed by adding the machine cycles for the tests together and then allowing proper compensation for the tests within the structure of the "counting down" technique. This is evident in the testing of the presence of the ISL59885 sync separator as a reference generator and therefore detecting the presence of a HDTV video signal and stop further signal processing or the detection of a SDTV video signal and proceed with the signal processing. Once the remainder of the first vertical serration has been completed and the second vertical pulse has been loaded into the appropriate outputs, the status of pin2, or PD0, of IC2 is tested. If the bit is "high", the input video signal is standard definition or SDTV and, at this point, may be any one of the four sync separators suggested for use in this project as a reference generator. If the bit is "low", the input video signal is high definition or HDTV and the ISL59885 sync separator is the reference generator.

Upon completion of the "counting down" of the last of the six post-equalizing

pulses, the program is directed to test the status of pin 9, or PD5, of IC2. This pin is connected to pin 7 of IC1, or the reference generator. In the cases of the LM1881 and the EL4581, pin 7 is the even/odd field output for both reference generators. A "high" status of this bit directs the program to the "ODD" label or the odd field subroutine. Upon completion of this subroutine, the program returns to "RESET". A "low" status of this bit directs the program to the "EVEN" label or the even field subroutine. Upon completion of this subroutine, the program returns to "RESET". In the cases of the EL1883 and the ISL59885, pin 7 is the horizontal output for both reference generators. Because the outputs of pin 7 are of standard horizontal sync pulse duration and in a proper time relation to the respective fields, the status of pin 7 coincides with the conditions of the program. The same "counting down" technique is implemented in the processing of both fields, upon the detection of each horizontal sync pulse with program directing the microcontroller to generate a corresponding horizontal sync pulse. When the "counting down" of the horizontal sync pulse is completed, the program then directs the microcontroller to generate the breezeway/burst pulse and the pulse-to-pulse interval pulse. The breezeway/burst pulse times out first, then the pulse-to-pulse interval pulse times out. This total amount of time approximates one line of the video signal and no other horizontal sync pulse is acknowledged by the microcontroller until this time has expired. The number of horizontal pulses is sequentially "counted down" to the end of the field of the detected format being processed and then the program returns to the "RESET" vector and therefore stays at the "LOOP" label until the next interrupt or vertical pulse.

The program of the ATtiny13 of the advanced version monitors the vertical sync pulse from the reference generators, but does not generate an interrupt. The detection of a vertical pulse starts a predetermined "counting down" of the duration of a NTSC field. If the status of the vertical output is low, the video signal input is of the NTSC format. This is because the PAL/SECAM formats have longer field durations and the status of the vertical output would be high. Once a single test has been made an output is generated. If the format is NTSC, the output is high and if the format is PAL/SECAM, the output is low. The program then generates a time delay of approximately 3.9 milliseconds to ensure the vertical pulses of any format tested have expired. The program then returns to the start of the program to await a vertical pulse. The program completes one full cycle every other field or once per frame and may begin at the "even" fields or the "odd" fields.

The comments to the right side of the semi-colons are to aid in the reading of the program by the experimenter by including references to the number of clock cycles being counted. These comments have no effect on the microcontroller or the program. This concludes the discussion of the programs.

Subsection C: Experimenter Exercises for Independent Study

Figure Four provides an approximation of the most critical waveforms. Table Four lists the test points and consists of a summation of the waveform sources, source operation (function), diagram reference and various comments. The waveforms provided are that of the NTSC SDTV standard.

Although the program is completely operational and it, like all programs, can

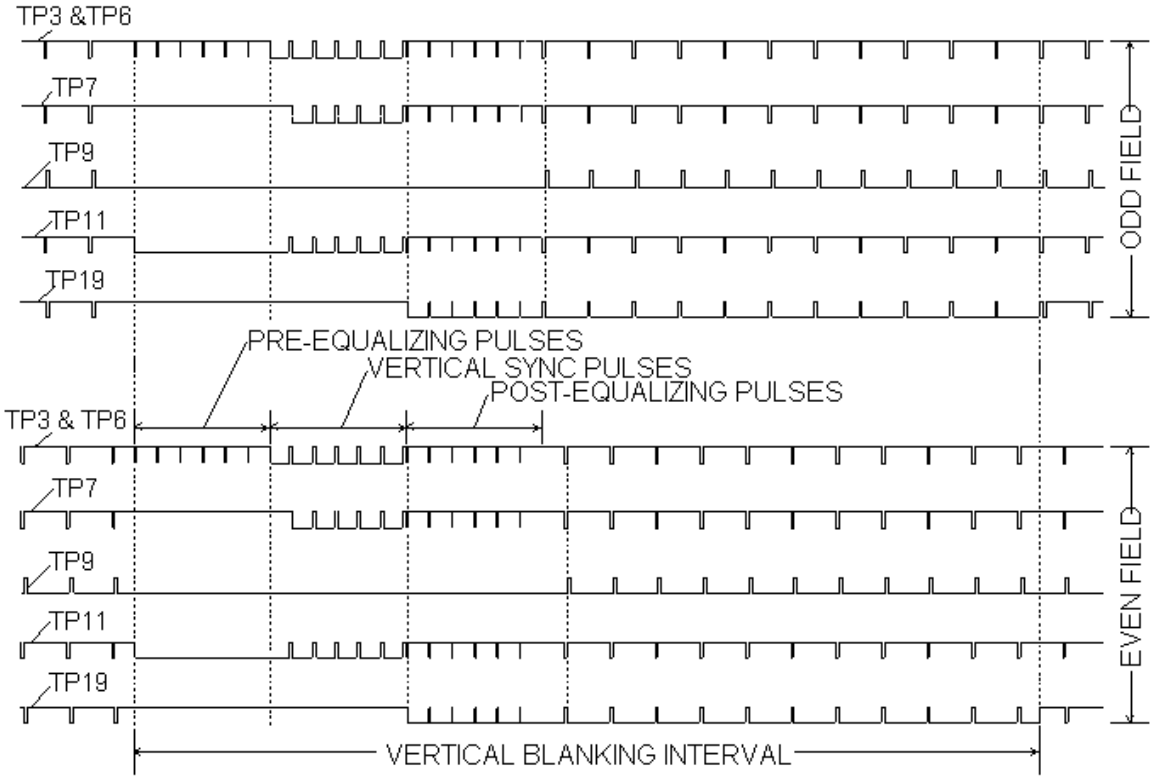


Figure Four

be "fine tuned" and/or modified. This dependent not only upon specified criteria as defined by the nature of the composite synchronizing signal standards, but also upon the experimenter's view of what the program should be able to do. This view may range from a degree of refinement to additional tasks other than the program dictates. This final section is presented in order to inspire and promote this type of attitude and reasoning. The following concepts and suggestions are intended as a precursor for independent exploration exercises. These exercises may have several solutions, each with its own particular advantage, and may be combined with others depending upon the desired flexibility and performance. Suggested topics of exploration include:

1.) Reducing the number of steps of the program is possible by making use of the other features of the ATtiny2313V. This requires a comprehensive review of the full datasheet, available from the Atmel website. Such features include the 128 bytes of EEPROM, one 8-bit timer and one 16-bit timer. Use of these features includes accessing and programming the proper registers and applying the associated instructions.

2.) Referring to the schematic diagram of the basic version, it is easily seen that the amount of amplifiers and gates can cause a cumulative propagation delay from the input to the output of the video signal. This delay does not become significant until it exceeds 0.5us or 500ns. In the case of these circuits, the basic version and the advanced version, the delay is approximately 0.45us (450ns) to 0.5us (500ns). There is a 40ns to 80ns delay of the horizontal sync pulse by the reference generator. There is a 50ns delay for each individual gate. This is clearly

TP	Signal Name	Source	Operation	Reference	Comments
1	Video Input			NA	Standard 1.0V p-p Video Signal
2	Vertical Sync Pulse	Reference Generator	ADC	Datasheet	Available on Website listed in Appendix
3	Composite Sync Signal	Reference Generator	ADC	Figure Four	Also Datasheet on Website
4	Even/Odd Field	Reference Generator	ADC	Datasheet	Available on Website listed in Appendix
5	HD/SD	Aux. Switch or Aux. uC	Program	NA	Either High or Low
6	Composite Sync Signal	Hybrid Sync Separator	ADC	Figure Four	May contain extraneous pulses
7	Horizontal Pulse	PB2 of Main uC	Program	Figure Four	
8	Modified #1 Sync	Series NAND Gates	AND	TP6*	TP6 & TP7 Logically Combined
9	Breezeway/Back Porch	PB3 of Main uC	Program	Figure Four	
10	Modified #2 Sync	Series NOR Gates	OR	TP6*	TP8 & TP9 Logically Combined
11	Pulse-to-Pulse Interval	PB4 of Main uC	Program	Figure Four	
12	Corrected Sync	Series NOR Gates	OR	TP6*	TP10 & TP11 Logically Combined**
13	Inverted Corrected Sync	NAND Gate Inverter	Invert	NA	Inverted Figure Two-NTSC
14	Error Pulses	Wired X-OR Gate	X-OR	NA	
15	Analog of TP13	Op-Amp Comparator	DAC	NA	Voltage-Limiting Conversion
16	Analog of TP14	Op-Amp Comparator	DAC	NA	Voltage-Limiting Conversion
17	Sync Corrected Video	Inserter/Stripper			Similar to TP1, but Sync Corrected
18	AGC Level	PB6 & PB7 of Main uC	Program	NA	Level is always low
19	AGC Insertion Timing	PB5 of Main uC	Program	Figure Four	Active Low -Mainly During VBI
20	AGC/Sync Regulated Video	DC-Restored Amplifier	DC-Restore		Similar to TP1; AGC/Sync Regulated

* Similarity depends upon the degree of signal degradation
** Corrected Sync Signal

Table Four

at the threshold the established limit. This propagation delay may be reduced to a nominal level by subtracting the delay of the reference generator and the delays of IC7a and IC7b. The reference generator delay should be 50ns or 100ns and the total of IC7a and IC7b would be 100ns.

3.) Instead of the ATtiny2313V waiting for a horizontal sync for each line, it is possible to create a program that would spontaneously generate a complete field pulse train when the vertical interrupt occurs and the standard and field are detected.

4.) In some cases, only the detection of and removal of extraneous sync signals and AGC regulation (DC restoration) may be desired. It is then not necessary to re-insert the majority of the composite sync pulse into the video signal being processed. Simple removal of IC9 will produce the desired result.

5.) The program of the ATtiny13 detects the video standard being processed by using the difference of field time between vertical sync pulses. That is the field of the NTSC standard has a longer duration than that of the PAL/SECAM standards. Is detection possible by using the difference between the vertical pulse durations? If so, this would implicate a much shorter real-time sampling of the video synchronizing signal. Is it then possible that such a program could be absorbed into the program of the ATtiny2313V and thereby eliminating the need for the ATtiny13?

6.) It is possible synthesize a slight advancing or retarding phase shift of the horizontal sync pulse. This would be limited to a fairly small amount for an NTSC SDTV video signal due to the color burst. Certain compensations may have to be incorporated to accomplish this. These compensations include decreasing the

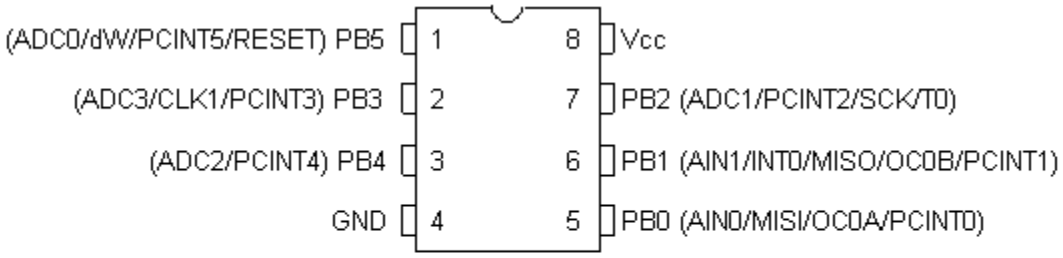
horizontal sync pulse duration in a phase advance operation or an increase in the breezeway (and therefore the entire back porch) duration for a phase retard operation. Another experimental application of this concept may be its application to analog R'G'B' signals. The major drawback is the requirement of additional regulator projects.

7.) It is possible write a program to encode a video signal as to render the resulting video display unintelligible without an accompanying regulator project with a decode program. This experimental encode/decode concept has possible uses in a closed circuit cable television systems from the private sector for security purposes to services in the public domain. The suggestion of radio frequency transmission and reception would have to be would have to be addressed with further experimentation. In the case of recording an encoded video signal and then decoding the video signal during playback, care must be taken not to corrupt the composite sync signal to the point where the recording/playback device(s) timing is adversely affected. This is because most recording/playback devices rely on the composite sync signal to synchronize the servo mechanisms of the units with the actual video signal processing and recording electronics.

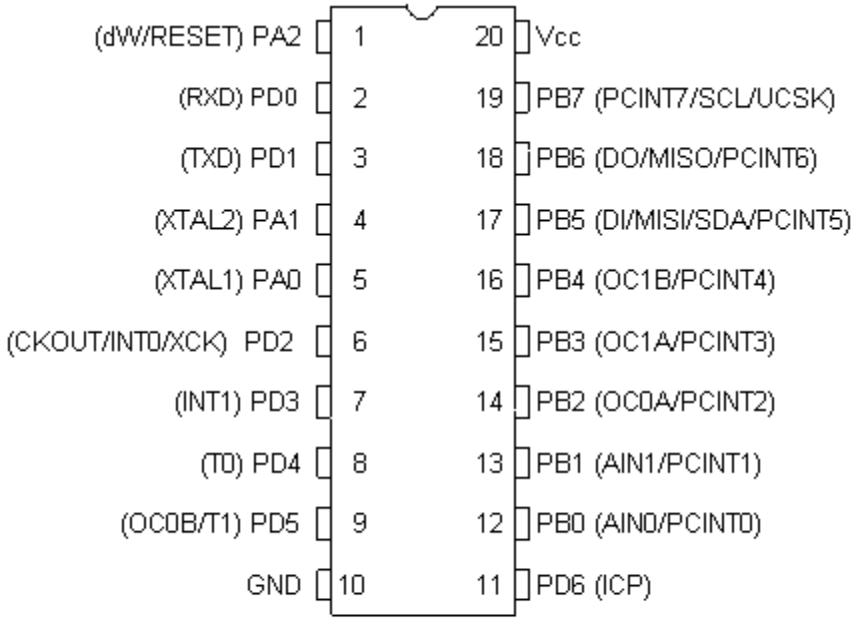
8.) After acquiring a complete LM1881 datasheet, it would be noticed that a video line selector circuit schematic is included. Since less than 50% of the program memory is used, a subroutine for line selection may be introduced to exclude that line from being processed. This is useful, for example, in the case of line 21 and line 284 of the NTSC standard in which closed captioning data resides. Widescreen signaling data is present online 20 and line 283 of the NTSC standard.

This concludes the manual for the "Microcontroller-Based Multi-Format Video AGC/Sync Loop Regulator". Any comments and/or constructive criticism would be greatly appreciated in order to improve the quality of this project. Please forward your comments to tronjohn@jlkelectronics.com or to:

J.L.K. Electronics
P.O. Box 0027
Blue Island, IL 60406-0027



Auxiliary uC



Main uC

Figure Five

APPENDIX

Suppliers/Vendors:

1. Digi-Key Corporation
   701 Brooks Ave. South
   Thief River Falls, MN 56701-0677
   Toll free orders: 1-800-344-4539
   www.digikey.com
2. All Electronics Corporation
   14928 Oxnard Street
   Van Nuys, CA 91411
   Toll free orders: 1-800-826-5432
   www.allelectronics.com
3. Avnet Electronics Marketing
   Corporate Headquarters
   2211 S. 47th Street
   Phoenix, AZ 85034
   1-800-332-8638
   www.em.avnet.com
4. Allied Electronics, Inc.
   7151 Jack Newell Blvd. S.
   Fort Worth, TX 76118
   1-866-433-5722
   www.alliedelec.com
5. Radio Shack Corporation
   Riverfront Campus
   Mailstop #CF3-311
   300 RadioShack Circle
   Fort Worth, TX 76102-1964
   1-800-THE-SHACK
   www.radioshackcorporation.com

Manufacturers:

1. Atmel Corporation
   2325 Orchard Parkway
   San Jose, CA 95131
   1-408-441-0311
   www.atmel.com
2. Burr-Brown (same as Texas Instruments)
   www.burrbrown.com
3. Intersil Corporation
   1001 Murphy Ranch Road
   Milpitas, CA 95035
   1-408-432-8888
   1-888-INTERSIL
   www.intersil.com

4. Texas Instruments
   Literature Response Center
   14950 F.A.A. Blvd.
   Ft. Worth, TX 76155
   1-800-477-8924
   www.ti.com
5. Zetex Inc.
   700 Veterans Memorial Highway
   Suite 315
   Hauppauge, NY 11788
   1-631-360-2222
   www.zetex.com

References and Suggested Reading

1. Keith Jack
   Video Demystified-4th Edition
   Newnes Publications, Burlington, MA 01803
   2005
   ISBN: 0-7506-7822-4
2. Keith Jack, Vladimir Tsatsulin
   Dictionary of Video and Television Technology
   Newnes Publications, Burlington, MA 01803
   2002
   ISBN: 1-878707-99-X
3. Rudolf F. Graf, William Sheets
   Video Scrambling & Descrambling for Satellite & Cable TV-2nd Edition
   Newnes Publications, Burlington, MA 01803
   1998
   ISBN: 0-7506-9997-3
4. Rudolf F. Graf
   Modern Dictionary of Electronics-7th Edition
   Newnes Publications, Burlington, MA 01803
   1999
   ISBN: 0-7506-9866-7
5. ***AVR RISC Microcontroller Data Book-August 1999***
   Atmel Corporation, San Jose, CA 95131
6. John Morton
   AVR An Introductory Course
   Newnes Publications, Burlington, MA 01803
   2002
   ISBN: 0 7506 56352
7. Bruce Carter,
   Video Designs Using High-Speed Amplifiers
   Texas Instruments Application Report SLOA057-November 2007
8. ***Timing and Synchronization in a Multi-Format Facility***
   Tektronix Application Note

9. John Lidgey, Chris Toumazou, Mink Wong
EL4089 and EL4390 DC Restored Amplifier
Elantec Application Note #6
10. Arild Rodland
Novice's Guide to AVR Development
Atmel Applications Journal
Atmel Corporation, San Jose, CA 95131
11. Eivind Sivertsen
Basic Interrupts and I/O
Atmel Applications Journal
Atmel Corporation, San Jose, CA 95131